IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

LISTING OF CLAIMS

We claim:

1. (original) An apparatus comprising:

descriptor logic, said apparatus for controlling flow of data between first and second data processing systems via a memory, said descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and

a pointer descriptor identifying the location in the memory; and

a descriptor table for storing the descriptors generated by the descriptor logic for access by the first and second data processing systems.

2. (original) An apparatus as claimed in claim 1, wherein the descriptor table is stored in the first data processing system.

3. (original) An apparatus as claimed in claim 1, wherein the descriptor table is stored in the second data processing system.

4. (original) An apparatus as claimed in claim 1, wherein the descriptor logic generates a branch descriptor comprising a link to another descriptor in the descriptor table.

5. (original) An apparatus as claimed in claim 4, wherein the descriptor table comprises a plurality of descriptor lists sequentially linked together via branch descriptors therein.

6. (original) An apparatus as claimed in claim 4, wherein the descriptor table comprises a cyclic descriptor list.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

7. (original) An apparatus as claimed in claim 1, wherein the first data processing system comprises a host computer system.

8. (original) An apparatus as claimed in claim 1, wherein the second data processing system comprises a data communications interface for communicating data between the host computer system and a data communications network.

9. (currently amended) A data processing system comprising:

a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, and

apparatus ~~as claimed in claim 1~~ comprising:

descriptor logic, said apparatus for controlling flow of data between first and second data processing systems via a memory, said descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and

a pointer descriptor identifying the location in the memory; and

a descriptor table for storing the descriptors generated by the descriptor logic for access by the first and second data processing systems, for controlling flow of data between the memory of the host computer system and the data communications interface

10. (original) A method comprising controlling flow of data between first and second data processing systems via a memory, the step of controlling comprising:

by descriptor logic, generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system,

a pointer descriptor identifying the location in the memory; and

storing the descriptors generated by the descriptor logic in a descriptor table for access by the first and second data processing systems.

11. (original) A method as claimed in claim 10, comprising storing the descriptor table in the first data processing system.

12. (original) A method as claimed in claim 10, comprising storing the descriptor table in the second data processing system.

13. (original) A method as claimed in claim 10, comprising, by the descriptor logic, generating a branch descriptor comprising a link to another descriptor in the descriptor table.

14. (original) A method as claimed in claim 13, comprising linking a plurality of descriptor lists together in series via branch descriptors to form the descriptor table.

15. (original) A method as claimed in claim 10, wherein the first data processing system comprises a host computer system.

16. (original) A method as claimed of claim 10, wherein the second data processing system comprises a data communications interface for communicating data between the host computer system and a data communications network.

17. (original) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing control of flow of data

between first and second data processing systems, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect the functions of claim 1.

18. (currently amended) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing data processing, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect the functions of ~~claim 9~~ a data processing system comprising:

a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, and

apparatus comprising:

descriptor logic, said apparatus for controlling flow of data between first and second data processing systems via a memory, said descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and

a pointer descriptor identifying the location in the memory; and

a descriptor table for storing the descriptors generated by the descriptor logic for access by the first and second data processing systems, for controlling flow of data between the memory of the host computer system and the data communications interface.

19. (currently amended) An article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing control of flow of data between first and second data processing systems, the computer readable program code means in said article of manufacture comprising computer readable program code means for causing a

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

computer to effect the steps of ~~claim 10~~ a method comprising controlling flow of data between first and second data processing systems via a memory, the step of controlling comprising:

by descriptor logic, generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system,

a pointer descriptor identifying the location in the memory; and

storing the descriptors generated by the descriptor logic in a descriptor table for access by the first and second data processing systems.

20. (currently amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for controlling flow of data between first and second data processing systems, said method steps comprising the steps of ~~claim 10~~ a method comprising controlling flow of data between first and second data processing systems via a memory, the step of controlling comprising:

by descriptor logic, generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system,

a pointer descriptor identifying the location in the memory; and

storing the descriptors generated by the descriptor logic in a descriptor table for access by the first and second data processing systems.